> "A fairly uniform standard for determining compliance with the "written description" requirement has been maintained throughout: "Although [the applicant] does not have to describe exactly the subject matter claimed,.....the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed." *Vas-Cath,* 19 USPQ2d at 1116.

The Federal Circuit then cited *In re Heinle,* 145 USPQ 131 (CCPA 1965), in support of its holding. *Vas-Cath,* 19 USPQ2d at 1118. The court in *In re Heinle* reiterated the following rule for amendments to the specification:

> "This is the familiar rule that the drawings and the specification may be amended to conform to each other and that the added matter will not be deemed technical "new matter" within the prohibition of the law. 35 USC 132." *In re Heinle,* 145 USPQ at 136.

The Present Application

The applicant respectfully submits that the figures and specification of the present application, as filed, clearly allow persons skilled in the art to recognize that the layer 215 is oxide. Furthermore, the amendment replacing the term "active area 215" on pages 4 and 5 with the term --oxide layer 215-- merely conforms the description of Figures 2A-2D with Figure 1, the description of Figure 1, and claims 9 and 11, and is not "new matter."

Original Figures 2A-2D show an electrode 205 over a layer 215 with a selective spacer 210 deposited only on the electrode 205 and not on the layer 215. The layer 215 was originally described as "active area 215" on page 4, line 27 and on page 5, lines 5-6 of the specification. The term "active area" is well known to those skilled in the art. An "active area" of an integrated circuit is a two-dimensional area, looking down on a layout of the integrated circuit, in which a device such as a transistor is formed. The "active area" is the area of the integrated circuit between isolating regions of field oxide that are formed to electrically insulate neighboring devices from each other. The applicant has previously filed selections from two textbooks that disclose the meaning of the term "active area" known to those skilled in the art. The selections were attached to the amendment filed April 9, 1999.

The first selection is Neil H. E. Weste & Kamran Eshraghian, *Principles of CMOS VLSI Design A Systems Perspective* (1985), pages 71-72. A thin oxide or thinox mask is described as defining where areas of thin oxide are needed to implement devices. The term active area is given as another name for the mask, which is shown on page 72 having rectangular areas

defining active areas for an integrated circuit.

The second selection is Lance A. Glasser & Daniel W. Dobberpuhl, *The Design and Analysis of VLSI Circuits* (1985), pages 4, 101-103, 176-179, 182, and 183. On page 4 the active area is described as including "regions of heavily doped single-crystal silicon and transistor gate area". On page 102 the active area device edge is described as being moved by field oxidation. An "active area mask is used to define a region to be blocked from field oxidation." In other words, an active area mask defines active areas and insulating areas of field oxide. On page 103 it is stated that "[i]n MOS technology, oxide thickness is the primary parameter used to distinguish active (transistor) areas from inactive (field) areas." Here is a direct association between a layer of oxide and an active area of an integrated circuit, the active area being defined by a thickness of the layer of oxide. It is therefore not incorrect to point to a layer of oxide and call it an active area. An active area mask is mentioned again on page 176 as defining "what will eventually be sources, drains, channels, and diffused cross unders." The remaining pages describe and illustrate the role of the active area mask.

The focus of the description is on the selective spacer 210 which is deposited *only* on the electrode 205 and *not* on the layer 215 because of the phenomenon shown in Figure 1. Figure 1 illustrates that a "deposition of spacer materials on polysilicon 110 occurs more rapidly than deposition on oxide 120....The difference in incubation time 130 on dissimilar materials makes selective spacer deposition possible." Specification page 4, lines 8-12. Later it is stated that "Figures 2A-2D show how this incubation time difference 130 can be exploited for selective spacer deposition." Specification page 4, lines 19-20. With reference to the process: "In the second step, represented in Figures 2B and 2C, a selective spacer 210 is deposited such that the amount deposited on the polysilicon and refractory metal of electrode 205 is less than the incubation thickness, leaving the active area 215 free of deposition." Specification page 4, lines 24-27. Looking at Figure 2B one skilled in the art could only conclude that the layer 215 is oxide. The use of the term "active area" to describe the oxide layer 215 is not incorrect because the oxide covers the "active area" in which the CMOS device is being formed. As mentioned above, a thickness of the oxide layer 215 defines what is the active area. Proceeding with the description: "Once the spacer is deposited, the device undergoes polycide reoxidation 220....active area 215 and selective spacers 210 are reoxidized 220." Specification page 5, lines

3-6. The layer of reoxidation 220 shown in Figure 2C implies to one skilled in the art the existence of an original layer of oxide - the oxide layer 215.

The original claims also provide support for the oxide layer 215. In claim 9, line 3, the act of forming an *insulating layer* on a semiconductor wafer is recited before the acts of forming an conductive layer and forming a gate by etching. Claim 11 recites a method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor wafer, an *insulating layer* disposed over the semiconductor layer, and a conductive layer disposed over the *insulating layer*, the method including the step of forming a gate having sidewalls exposing the conductive layer and some portion of the *insulating layer*. One skilled in the art would recognize that, according to claims 9 and 11, the gate is formed over the insulating layer. Oxide is known as the most common insulating layer in semiconductor devices.

Finally, one skilled in the art will understand that the oxide layer 215 is necessary for the CMOS device to function. MOS transistor structures are defined by a source region and a drain region implanted in a substrate or an epitaxial layer on either side of a gate electrode, the gate electrode being insulated by a layer of gate oxide from a channel region in the substrate between the source and drain regions. The embodiment of the invention described in the application is a gate structure for a CMOS device. In Figures 2A-2D one skilled in the art will recognize that the layer 215 must be oxide to be consistent with what is known about gate structures in CMOS devices. A source region and a drain region are not shown because they are not necessary to a description of the embodiment of the invention which is, primarily, the selective spacer 210 that is deposited on the electrode 205 and not on the oxide layer 215. The applicant agrees with the statement of the Examiner in paragraph 11 of the Final Office Action mailed April 27, 1999, that "[i]t is well known in the art that gate oxide separates and insulates the active areas from the gate electrode."

Therefore the applicant respectfully submits that the figures and specification of the present application, as filed, clearly allow persons skilled in the art to recognize that the layer 215 is oxide. Furthermore, the amendment replacing the term "active area 215" on pages 4 and 5 with the term --oxide layer 215-- merely conforms the description of Figures 2A-2D with Figure 1, the description of Figure 1, and claims 9 and 11, and is not "new matter."

Rejections under 35 USC §112

Claims 23-31 and 36-44 were rejected under 35 USC § 112, first paragraph. The applicant respectfully traverses.

As discussed above the layer 215 shown in Figures 2A-2D is an oxide layer. The oxide layer 215 is now explicitly recited in the specification.

Regarding claims 23-25, claim 23 recites a semiconductor device including, among other elements, an oxide layer, at least one feature having a surface and being contiguous with the oxide layer at a boundary, and a spacer covering a surface of the feature and terminating at the boundary wherein the spacer is not in contact with the oxide layer. Support for this limitation is found in Figures 2B and 2C and in the specification where it is described that the spacer 210 is deposited on the electrode 205 and not on the oxide layer 215. Page 4, lines 25-28.

Claims 26-31, 36-41 and 44 were rejected under 35 USC § 112, first paragraph. The applicant respectfully traverses. As discussed above the layer 215 shown in Figures 2A-2D is an oxide layer. The oxide layer 215 is now explicitly recited in the specification.

Claims 26-31, 36-41, and 44 were rejected under 35 USC § 112, second paragraph. The applicant respectfully traverses. As discussed above the layer 215 shown in Figures 2A-2D is an oxide layer. The oxide layer 215 is now explicitly recited in the specification.

Rejection under 35 U.S.C. §103

Claims 23, 25-27, 29, 30, 36, 38, 42, and 44 were rejected under 35 USC § 103(a) as being unpatentable over Ho et al. (U.S. Patent No. 5,364,804, Ho) and Keller et al. (U.S. Patent No. 5,707,898, Keller) in view of Manning (U.S. Patent No. 5,804,838) or McLevige (U.S. Patent No. 4,711,701). The applicant respectfully traverses.

Keller issued on January 13, 1998, and Manning issued on September 8, 1998, both issue dates being after the filing date of the present application. The applicant does not admit that either Keller or Manning is prior art, and reserves the right to swear behind Keller or Manning at a later date.

Claim 23 recites, among other elements, an oxide layer, at least one feature over the oxide layer having a surface, and a spacer comprising silicon nitride or an amorphous silicon film

covering the surface of the feature and terminating at a boundary wherein the spacer is not in contact with the oxide layer.

Ho is deficient in the following respects. Ho discloses in Figures 9 and 10 a layer 26 of oxide on sidewall of a gate electrode. Ho also discloses a silicon nitride layer 28 overlaying the oxide layer 26, and this is shown with particularity in Figure 9. In column 3, lines 46-48, Ho describes the purpose of the silicon nitride layer 28 as to provide a more vertical sidewall than the oxide layer 26. Ho does not disclose the spacer comprising silicon nitride or an amorphous silicon film that is not in contact with the oxide layer as recited in claim 23. In fact, the very purpose of the silicon nitride layer 28 of Ho is to be in contact with the oxide layer 26 to correct for the non-vertical surface of the oxide layer 26.

Keller does not supply the elements missing in Ho. Keller discloses in Figure 2 a gate construction 16a with "outer sidewalls 23 having an oxide layer 24 grown thermally thereover." Column 3, lines 2-3. Furthermore, the gate construction 16a includes "sidewall spacers 26, typically comprising undoped SiO_2" or silicon dioxide. Column 3, lines 20-22. Therefore the layer 24 and the spacers 26 on the gate construction 16a are both oxide, and therefore Keller clearly does not show the spacer comprising silicon nitride or an amorphous silicon film that is not in contact with the oxide layer as recited in claim 23.

Manning does not supply the elements missing in Ho and Keller. Manning discloses in Figure 10 silicon nitride spacers 48 and 50 on a silicon material 14 and in contact with a layer of oxide 13. Manning does not disclose the spacer comprising silicon nitride or an amorphous silicon film that is not in contact with the oxide layer as recited in claim 23.

Finally, McLevige does not supply the elements missing in Ho, Keller, and Manning. McLevige discloses in Figures 2d, 3c, and 4b sidewall deposits of SiO_2 64 that are deposited on TiW 142 and an underlying layer of silicon nitride 38. McLevige states in column 5, lines 18-20, that "[i]n the case that the silicon nitride layer is omitted, the silicon dioxide could be replaced by silicon nitride." However, there is no indication that, in making this statement, McLevige is referring to the sidewall deposits of SiO_2 64 and the layer of silicon nitride 38. Therefore, McLevige does not disclose the spacer comprising silicon nitride or an amorphous silicon film that is not in contact with the oxide layer as recited in claim 23.

Furthermore, there must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17. The Examiner has not identified any statements or other evidence in the applied references that is a clear and particular teaching to combine the references.

Therefore, even as combined, Ho, Keller, Manning, and McLevige do not disclose or suggest all the elements recited in claim 23, or in claim 25 which is dependent on claim 23. The applicant respectfully submits that claims 23 and 25 are in condition for allowance.

Claims 26, 27, 29, 30, 36, 38, 42, and 44 recite elements similar to the elements recited in claims 23 and 25. For reasons analogous to those stated above with respect to claim 23, and the limitations in the claims, the applicant respectfully submits that claims 26, 27, 29, 30, 36, 38, 42, and 44 are not disclosed or suggested by the combination of references put forward by the Examiner, and that claims 26, 27, 29, 30, 36, 38, 42, and 44 are in condition for allowance.

Claims 24, 28, 31, 37, 39-41, and 43 were rejected under 35 USC § 103(a) as being unpatentable over Ho, Keller, Manning, and McLevige as applied above, and further in view of Gonzalez (U.S. Patent No. 5,608,249). The applicant respectfully traverses.

Gonzalez issued on March 4, 1997, which is less than one year before the filing date of the present application. The applicant does not admit that Gonzalez is prior art, and reserves the right to swear behind Gonzalez at a later date.

Claims 24, 28, 31, 37, and 43 are dependent on the claims discussed above. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 24, 28, 31, 37, and 43 are not disclosed or suggested by the combination of references put forward by the Examiner, and that claims 24, 28, 31, 37, and 43 are in condition for allowance.

Claims 39-41 recite elements similar to the elements recited in claim 23. Gonzalez does not supply the elements missing in the other applied references as discussed above with respect to claim 23. For reasons analogous to those stated above with respect to claim 23, and the limitations in the claims, the applicant respectfully submits that claims 39-41 are not disclosed or

suggested by the combination of references put forward by the Examiner, and that claims 39-41 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KLAUS FLORIAN SCHUEGRAF ET AL.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on **December 28, 1999**.

Tina Pugh
Name

_____
Signature